CLAIM STATUS AND AMENDMENTS

1-9. (cancelled)

10. (withdrawn) A method of producing a cell, having multibit storage, comprising: forming on a semiconductor surface a thin layer of tunnel oxide; depositing on said tunnel oxide a metal wetting film; annealing the film to produce self-assembled nanocrystals on said tunnel oxide; depositing a control oxide layer on said nanocrystals; forming a control gate on said control oxide layer; implanting said semiconductor surface to form self-aligned source and drain regions; and supplying reversible source-to-drain bias voltages for asymmetrically charging first and second portion of said nanocrystals near said source and drain regions, respectively.

11. (withdrawn) The method of claim 10, wherein supplying said bias voltages includes supplying first and second write bias voltages to said source and drain for writing information to said first portion of said nanocrystals and reversing said first and second write bias voltages for writing information to said second portion of said nanocrystals.

12. (withdrawn) The method of claim 10, wherein supplying said bias voltages further includes supplying first and second read bias voltages to said source and drain for reading information written to said first portion of said nanocrystals and reversing said first and second read bias voltages for reading information written to said second portion of said nanocrystals.

13. (new) A multibit storage cell, comprising:

a semiconductor substrate having source and drain regions separated by a channel region;

an insulator material formed on said substrate and having a plurality of metal nanocrystals embedded therein, said metal nanocrystals including a first portion forming a first storage element located in the region of a source side junction with said channel and a second portion forming a second storage element located in the region of a drain side junction with said channel;

a gate electrode on said insulator material;

a control layer formed in said insulator material between said gate electrode and said metal nanocrystals;

a tunnel layer formed between said metal nanocrystals and said substrate; and

bias voltages connected to said source and drain regions to produce asymmetric charging of said nanocrystals, wherein said metal nanocrystals are formed from a metal that is selected to have a work function value which affects transport of charge through said insulating material such that a first, low potential barrier is formed across said tunnel oxide during writing to said storage elements, and a second, higher potential barrier is formed across said tunnel oxide during retention of charge in said storage elements.

14. (new) The storage cell of claim 13, wherein said gate electrode overlies said nanocrystals and said channel.

15. (new) The storage cell of claim 13, wherein said bias voltages are connected to write and to read multiple bits of data in said storage elements.

16. (new) The storage cell of claim 15, wherein said bias voltages include write voltages selected to independently write data to said first and second storage elements.

17. (new) The storage cell of claim 15, wherein said bias voltages include read voltages selected to independently read data from said first and second storage elements.

18. (new) The storage cell of claim 15, wherein said bias voltages include first and second write voltages connectable to said source and drain to write information to said first storage element, and being reversible to write information to said second storage element.

19.(new) The storage cell of claim 17, wherein said bias voltages further include first and second read voltages connectable to said source and drain to read information written to said first storage element, and reversible to read information written to said second storage element.